Patent claims

1. A high-voltage PMOS transistor having an insulated gate electrode (18), a p-conductive source region (15) in an n-conductive well (11), a p-conductive drain region (14) in a p-conductive well (12) which is arranged in the n well, and having a field oxide area (13) between the gate electrode and drain region, the depth (A'-B') of the n-conductive well underneath the drain region (14) being less than underneath the source region (15), and the depth (A'-C') of the p-conductive well being greatest underneath the drain region (14).

2. The high-voltage PMOS transistor as claimed in claim 1, characterized in that the p-conductive well (12) extends laterally from the drain to the gate electrode (18).

3. The high-voltage PMOS transistor as claimed in claim 1 or 2, characterized in that the gate electrode (18) extends above an insulating layer (17) from the source region (15) as far as the field oxide (13) in the direction of the drain so that it covers the edge areas of the p-conductive well (12).

4. The high-voltage PMOS transistor as claimed in one of claims 1 to 3, characterized in that a metal layer (19) extends at a predefined distance above the field oxide (13) and is connected to the gate electrode (18) by means of a via (20), and in that the metal layer extends over the field oxide area from the gate electrode in the direction of the drain.

5. The high-voltage PMOS transistor as claimed in one of claims 1 to 4, characterized in that the p-conductive well (12) is more highly doped in the vicinity of the drain (14) than in the external area towards the transistor channel (K).

6. The high-voltage PMOS transistor as claimed in one of claims 1 to 5, characterized in that the n-conductive well (11) has lower doping underneath the drain than in the area underneath the transistor channel.

7. A mask for manufacturing an n-conductive well, in particular for a high-voltage PMOS transistor as claimed in one of claims 1 to 6, in which the area of the drain which is provided is covered with a drain cover (21).

8. The mask as claimed in claim 7, characterized in that a further cover (22) between the areas which are provided for the drain and the source is produced at a distance from the drain cover (21).

9. The mask as claimed in claim 8, characterized in that the further cover (22) is embodied in a strip shape.

10. The mask as claimed in one of claims 7 to 9, characterized in that the drain cover (21) is firstly widened in the vicinity of the transistor head (TK) and then tapers.

11. The mask as claimed in one of claims 7 to 10, characterized in that the drain cover (21) extends in an arc in the vicinity of the transistor head (TK).

12. The mask as claimed in one of claims 8 to 11, characterized in that the further cover (22) follows the profile of the drain cover in the vicinity of the transistor head, at a distance.

13. A masking for manufacturing a p-conductive well (12), in particular for a high-voltage PMOS transistor

as claimed in one of claims 1 to 6, in which additional covers (24, 25) are provided in certain sections between the central area (Z) and the edge area of the well which is to be produced.

14. The masking as claimed in claim 13, characterized in that the additional covers contain conically extending strips (24) which widen from the source-side edge area to the drain-side area and are spaced apart from one another.

15. The masking as claimed in claim 13 or 14, characterized in that the additional covers (25) are formed in the vicinity of the transistor head as strips which are spaced apart from one another.

16. The masking as claimed in claim 14, characterized in that the strip-shaped additional covers are a plurality of strips which extend in an arc.

17. The masking as claimed in claim 14 or 16, characterized in that the strips extend in parallel at least in certain sections.

18. A method for manufacturing an n-conductive well (11) and a p-conductive well (12), in particular when manufacturing a high-voltage PMOS transistor as claimed in one of claims 1 to 6, in which the implantation of ions is carried out by means of masks or maskings in such a way that the depth of the n well is less in the area of the drain which is provided than in the other well areas.

19. The method as claimed in claim 18, characterized in that the local conductivity of the p-conductive well is also determined by the doping of the n-conductive well.

20. The method as claimed in claim 18 or 19, characterized in that the well masking is carried out for the p-conductive well in such a way that the doping depth of the p-conductive well in the drain region which is provided is greater than in the direction of the areas which are assigned to the source.